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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,141	08/27/2004	Shiao-Shien Chen	NAUP0623USA	5140

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EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,141	CHEN, SHIAO-SHIEN	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Ker et al., Publication No. 2002/0181177A1. With respect to claims 1 and 12, applicant's prior art (Fig. 1 and Fig. 2) teaches a substrate-triggered ESD protection circuit 10, which is formed on a P-type substrate 12 and comprises a first power terminal VDD; a second power terminal VSS; a resistor R connected to the first power terminal VDD; a capacitor C connected between the resistor R and the second power terminal VSS; a first p+ diffusion region 22 in the P-type substrate 12 connected to the second power terminal VSS; an N-well 20 in the P-type substrate 12; a first n+ diffusion region 16 in the N-well connected to the first power terminal VDD; and an ESD detecting circuit connected to the first power terminal VDD having an input terminal connected to the resistor R and the capacitor C and a output terminal connected to the p+ diffusion region, wherein the output terminal outputs signal opposite to signal received by the input terminal so as to change a voltage level of the P-well as disclosed in Fig. 1 and Fig. 2.

However, the prior art fails to teach or suggest a P-well in the N-well, at least a second p+ diffusion region in the P-well, at least a second n+ diffusion region in the P-well connected to the first power terminal, and at least third n+ diffusion region in the P-well connected to the second power terminal.

Ker et al. teaches an electrostatic discharge protection circuit using deep N-well structure. Ker et al. teaches a P-well 84 in the N-well 88, at least a second p+ diffusion region in the P-well, at least a second n+ diffusion region in the P-well connected to the pad 64, and at least third n+ diffusion region in the P-well connected to the second power terminal VSS as disclosed in Fig. 11.

Both teachings are related by being electrostatic discharge protection circuits that use triple-well structure. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ker et al., which teaches a P-well in the N-well, into the ESD protection circuit of the applicant's acknowledged prior art because a deep N-well is often added into the CMOS processes to reduce noise coupling through common p-type substrate, to meet the required circuit specifications, and to support the IC design for high-integration applications.

Claim 11 differs from claim 1 by having an n-p-n bipolar junction transistor formed in the P-well, wherein an equivalent circuit between a base and a emitter of the BJT is a diode without connecting to any resistor in parallel. Ker et al. teaches a P-well 84 in the N-well 88, wherein there is at least an NMOS transistor Mn6 in the P-well. It is well known in the art that a diode-equivalent

model exists between the emitter and base PN junctions of an n-p-n BJT transistor, without the need for an external resistor connected in parallel, and there are many electronic devices in use today that make use of this effect.

With respect to claim 2, it is well known in the art to have a normal operation of protection transistor in response to a positive pulse of an ESD event. The positive ESD event is explained as being handled via a PN junction forming between the P-well and the third n+ diffusion region.

With respect to claim 3, Ker et al. teaches that there is at least an NMOS transistor Mn6 in the P-well 84, a drain of the NMOS transistor is the second n+ diffusion region, a source of the NMOS transistor is the third n+ diffusion region, and a body of the NMOS transistor is the P-well 84 as disclosed in Fig. 11.

With respect to claims 4 and 14, applicant's prior art teaches that the gate of the NMOS transistor 36 is connected to the second power terminal VSS as disclosed in Fig. 2.

With respect to claims 5 and 15, applicant's prior art teaches that the gate of the NMOS transistor is connected to the output terminal of the ESD detecting circuit as disclosed in Fig. 4.

With respect to claims 6, 13 and 16, Ker et al. teaches that there is at least an NMOS transistor Mn6 formed in the P-well 84, a drain of the NMOS transistor is the second n+ diffusion region, a source of the NMOS transistor is the third n+ diffusion region, and a body of the NMOS transistor is the P-well 84. It is well known in the art that a parasitic n-p-n bipolar junction transistor (BJT) is always

formed with the NMOS transistor, which is formed in the P-well 84. Therefore, a collector of the BJT is the second n+ diffusion region, a base of the BJT is the P-well, and a emitter of the BJT is the third n+ diffusion region.

With respect to claims 7 and 17, applicant's prior art teaches that the ESD detecting circuit is an inverter 30 as disclosed in Fig. 2.

With respect to claims 8 and 18, applicant's prior art teaches that the ESD detecting circuit is a PMOS transistor because one of the MOS's in the inverter-ESD detecting circuit 30 is a PMOS transistor as disclosed in Fig. 2.

With respect to claims 9 and 19, applicant's prior art teaches that the second p+ diffusion region 14 is positioned between two of the second n+ diffusion regions 16 as disclosed in Fig. 1.

With respect to claims 10 and 20, the second n+ diffusion region and the third n+ diffusion region being surrounded by the second p+ diffusion region simply represents a polarity reversal of regions already described in claim 9 above.

2. ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
10/31/2005

PHUONG T. VU
PRIMARY EXAMINER